



Dynamic dv/dt Rating

175 Operating Temperature

Fast Switching

Ease of Paralleling

Simple Drive Requirements

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

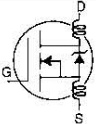
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_c=25$	Continuous Drain Current, $V_{GS}@ 10V$	10	A
$I_D @ T_c=100$	Continuous Drain Current, $V_{GS}@ 10V$	7.2	
I_{DM}	Pulsed Drain Current	40	
$P_D @ T_c=25$	Power Dissipation	43	W
	Linear Derating Factor	0.29	W/
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy	47	mJ
dv/dt	Peak Diode Recovery dv/dt	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

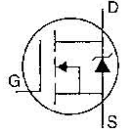
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	-	-	3.5	/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	-	0.50	-	
$R_{\theta JA}$	Junction-to-Ambient	-	-	62	

Electrical Characteristics @ T_J=25 (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	-	-	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	-	0.063	-	V/	Reference to 25 °C, I _D =1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	-	-	0.20	Ω	V _{GS} =10V, I _D =6.0A
V _{GS(th)}	Gate Threshold Voltage	2.0	-	4.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	2.4	-	-	S	V _{DS} =25V, I _D =6.0A
I _{DSS}	Drain-to-Source Leakage Current	-	-	25	μA	V _{DS} =60V, V _{GS} =0V
		-	-	250		V _{DS} =48V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-Source Forward Leakage	-	-	100	nA	V _{GS} =20V
	Gate-to-Source Reverse Leakage	-	-	-100		V _{GS} =-20V
Q _g	Total Gate Charge	-	-	11	nC	I _D =10A V _{DS} =48V V _{GS} =10V See Fig. 6 and 13
Q _{gs}	Gate-to-Source Charge	-	-	3.1		
Q _{gd}	Gate-to-Drain ("Miller") Charge	-	-	5.8		
t _{d(on)}	Turn-Off Delay Time	-	10	-	nS	V _{DD} =30V I _D =10A R _G =24Ω R _D =2.7Ω See Figure 10
t _r	Fall Time	-	50	-		
t _{d(off)}	Internal Drain Inductance	-	13	-		
t _f	Fall Time	-	19	-		
LD	Internal Drain Inductance	-	4.5	-	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
Ls	Internal Source Inductance	-	7.5	-		
C _{iss}	Input Capacitance	-	300	-	pH	V _{GS} =0V V _{DS} =25V f=1.0MHz See Figure 5
C _{oss}	Output Capacitance	-	160	-		
Cr _{ss}	Reverse Transfer Capacitance	-	29	-		

Source-Drain Ratings and characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	-	-	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)	-	-	40		
V _{SD}	Diode Forward Voltage	-	-	1.6	V	T _J =25 °C, I _S =10A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	-	70	140	ns	T _J =25 °C, I _F =10A
Q _{rr}	Reverse Recovery Charge	-	0.20	0.40	μC	di/dt=100A/μA
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

 V_{DD}=25V, starting T_J=25 °C, L=548μH, R_G=25Ω, I_{AS}=10A (See Figure 12)

 I_{SD}≤10A, di/dt ≤ 90A/μs, V_{DD}≤V_{(BR)DSS}, T_J≤ 175 °C

Pulse width ≤ 300μs; duty cycle ≤ 2%.

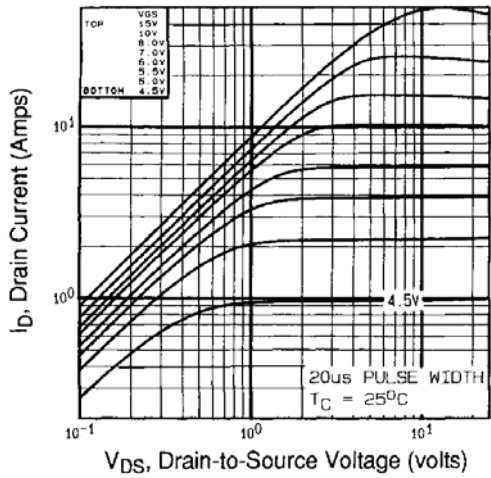


Fig 1. Typical Output Characteristics,
 $T_c=25$

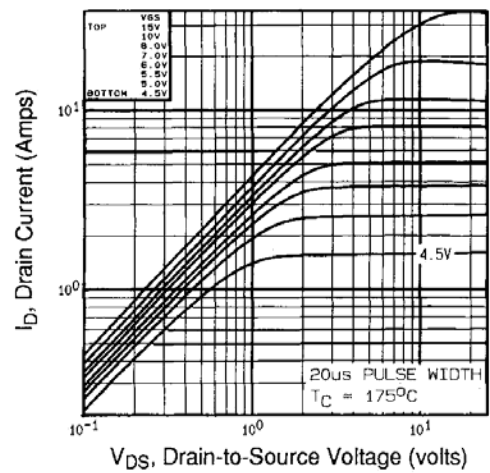


Fig 2. Typical Output Characteristics,
 $T_c=175$

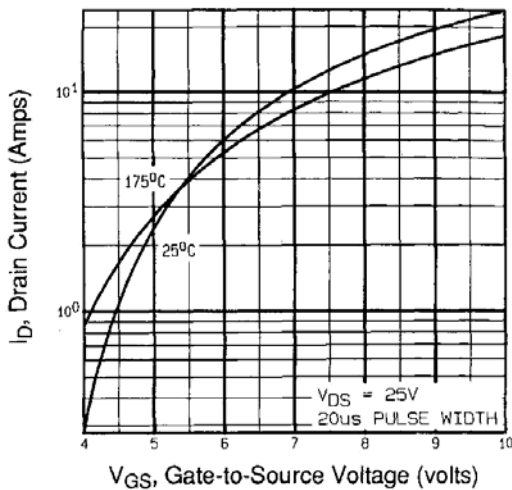


Fig 3. Typical Transfer Characteristics

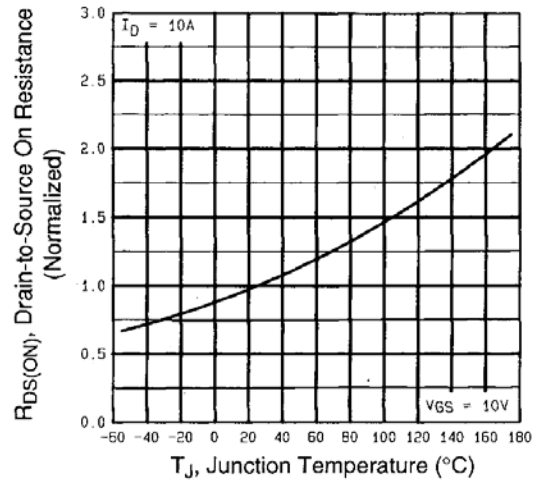


Fig 4. Normalized On-Resistance
Vs. Temperature

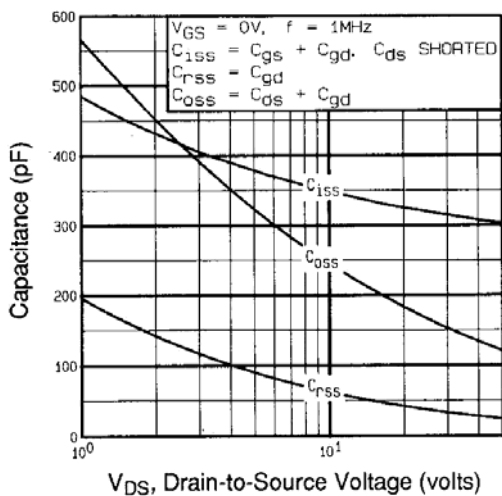


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

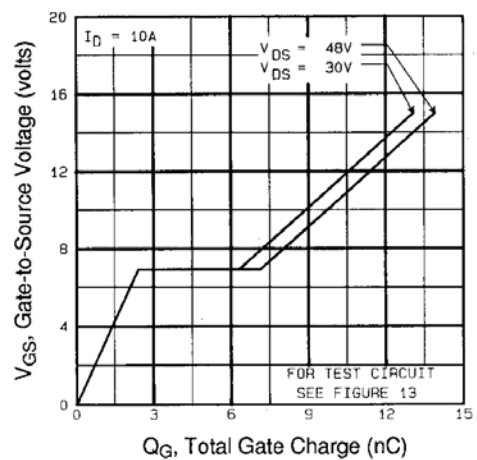


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

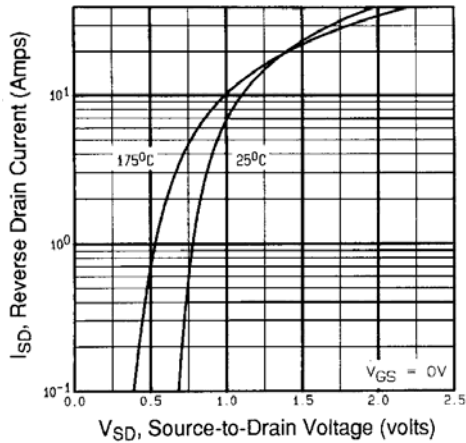


Fig 7. Typical Source-Drain Diode Forward Voltage

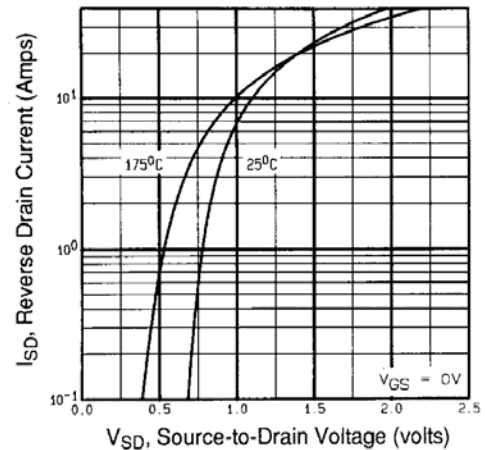


Fig 8. Maximum Safe Operating Area

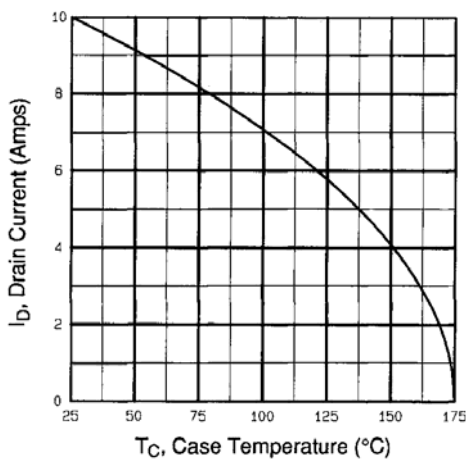


Fig 9. Maximum Drain Current Vs. Case Temperature

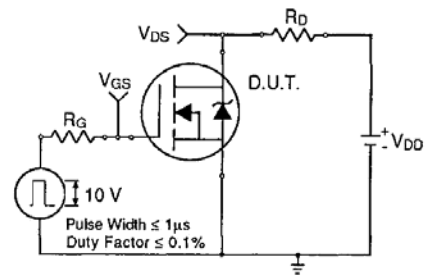


Fig 10a. Switching Time Test Circuit

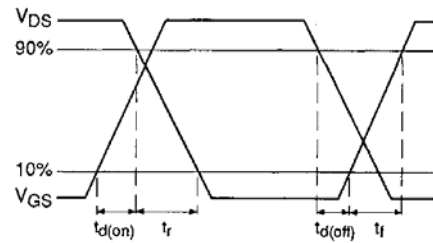


Fig 10b. Switching Time Waveforms

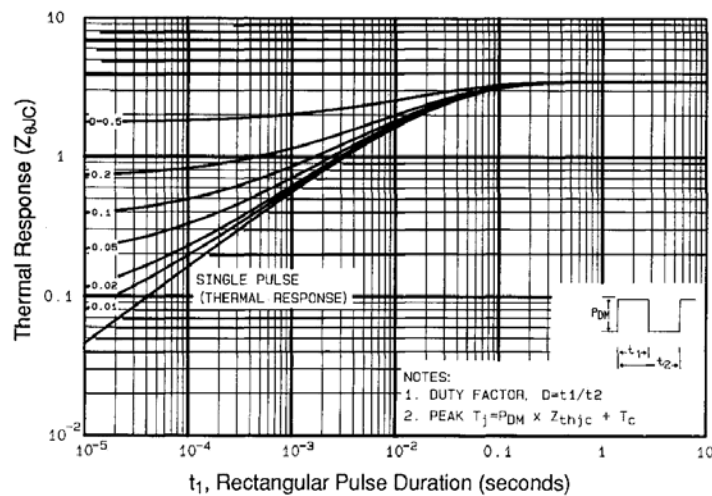


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

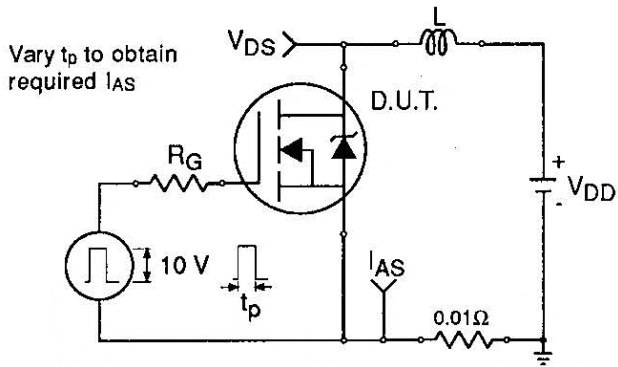


Fig 12a. Unclamped Inductive Test Circuit

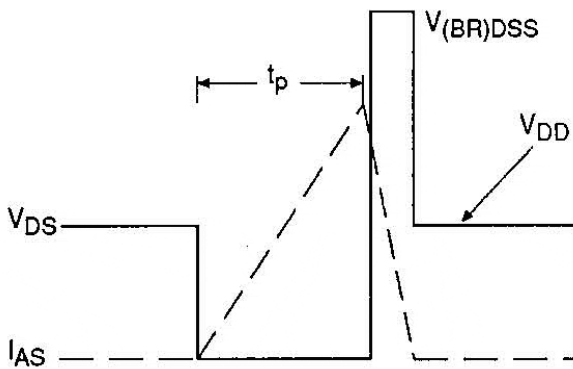


Fig 12b. Unclamped Inductive Waveforms

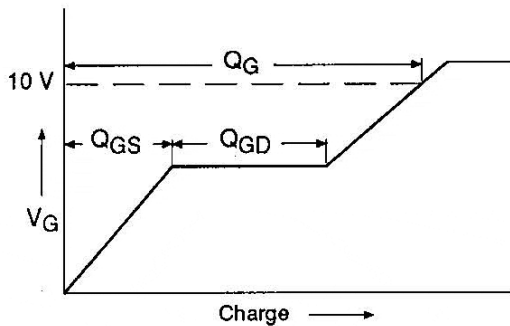


Fig 13a . Basic Gate Charge Waveform

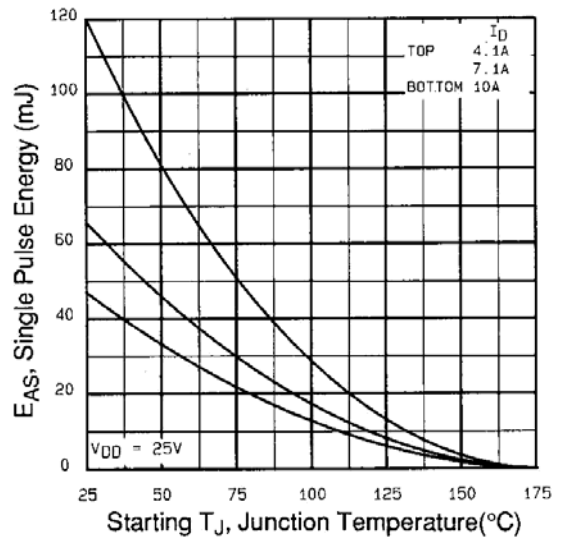


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

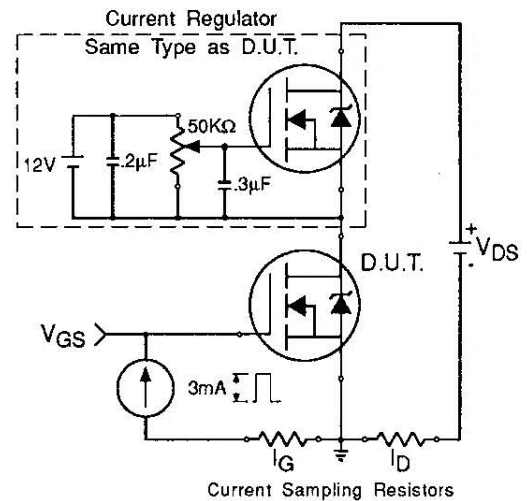


Fig 13b. Gate Charge Test Circuit